CLAIMS

I claim:

1. A method for fabricating an extended drain region of a high-voltage transistor comprising:

forming an epitaxial layer on a substrate, the epitaxial layer being of a first conductivity type and having a top surface;

etching the epitaxial layer to form a pair of spaced-apart trenches that define a mesa with first and second sidewall portions;

forming a dielectric layer in each of the trenches, the dielectric layer partially filling each of the trenches and covering the first and second sidewall portions;

filling a remaining portion of the trenches with a conductive material to form first and second field plate members that are insulated from the substrate and the epitaxial layer.

2. The method of claim 1 further comprising:

forming a source region of the first conductivity type at the top surface of the epitaxial layer, the extended drain region being defined between the source region and the substrate.

3. The method of claim 2 further comprising:

forming a source electrode connected to the source region and a drain electrode connected to the substrate.

4. The method of claim 1 wherein the dielectric layer and the field plate members are formed with a reduced spacing between the field plate members and the epitaxial layer near the top surface of the epitaxial layer as compared to near the substrate.

5. The method of claim 1 wherein the first conductivity type is n-type.

6. The method of claim 1 wherein the mesa has a lateral width that is less than 20% of a depth of the trenches.

7. The method of claim 1 wherein a doping concentration of the epitaxial layer is lower near the top surface as compared to near the substrate.

8. The method of claim 7 wherein the epitaxial layer is formed with a linearly graded doping profile.

9. The method of claim 1 wherein the dielectric layer comprises silicon dioxide.

10. The method of claim 1 wherein the field plate members comprise doped polysilicon.

11. The method of claim 3 further comprising:
thinning the substrate prior to formation of the drain electrode.

12. The method of claim 1 wherein the substrate is of the first conductivity type.

13. The method of claim 1 wherein the trenches extend through the epitaxial layer into the substrate.

14. The method of claim 1 wherein the dielectric layer has a lateral width that is greater than a lateral width of the mesa.

15. A method for fabricating a high-voltage transistor comprising:

forming an epitaxial layer on a substrate, the epitaxial layer being of a first conductivity type and having a top surface;

forming source and body regions in the epitaxial layer, the source region being of the first conductivity type and disposed at the top surface of the epitaxial layer, the body region being of a second conductivity type opposite to the first conductivity type;

forming a pair of spaced-apart trenches in the epitaxial layer that define a mesa with first and second sidewall portions;

forming a dielectric layer in each of the trenches that covers the first and second sidewall portions;

forming field plate members in the trenches, the field plate members comprising a conductive material that is insulated from the mesa; and

forming an insulated gate member between each of the field plate members and the mesa, a channel being defined adjacent the insulated gate member in the mesa across the body region.

16. The method of claim 15 further comprising:

forming source, gate, and field plate electrodes that connect with the source region, gate members, and field plate members, respectively.

17. The method of claim 15 wherein the first conductivity type is n-type.

18. The method of claim 15 wherein the epitaxial layer has a linearly graded doping profile.

19. The method of claim 15 wherein a doping concentration of the epitaxial layer is lower near the top surface as compared to near the substrate.

20. The method of claim 15 wherein the body region has a thickness in the approximate range of 0.5 – 3.0 microns.

21. The method of claim 15 wherein the dielectric layer and the field plate members are formed with a reduced spacing between the field plate members and the mesa near the top surface of the epitaxial layer as compared to near the substrate.

22. The method of claim 15 wherein the mesa has a lateral width that is less than 20% of a depth of the trenches.

23. The method of claim 15 wherein the dielectric layer comprises silicon dioxide.

24. The method of claim 15 wherein the dielectric layer has a lateral width that is greater than a lateral width of the mesa.

25. A method of fabricating a high-voltage transistor on a substrate, the method comprising:

forming a plurality of parallel arranged drift regions oriented in a first direction, each of the drift regions comprising a doped semiconductor layer of a first conductivity type interleaved with an insulating layer and a conducting layer, the conducting layer being insulated from the doped semiconductor layer by the insulating layer, the conducting layer comprising a field plate member of the high-voltage transistor;

forming source and body regions, the source region being of the first conductivity type and the body region b ing of a second conductivity type opposite to the first conductivity type, the body region separating the source region from the drift regions; and

forming an insulated gate adjacent the body region, the insulated gate defining a channel in the body region between the source region and the drift regions.

26. The method of claim 25 further comprising:

forming a drain region of the first conductivity type connected to the doped semiconductor layer of each of the drift regions.

27. The method of claim 25 wherein the substrate is of the first conductivity type.

28. The method of claim 26 further comprising:

forming a drain electrode coupled to the drain region; and

forming a source electrode coupled to the source region.

29. The method of claim 25 wherein the first conductivity type is n-type.

30. The method of claim 25 wherein the substrate has a planar bottom surface, with the first direction being oriented substantially parallel to the planar bottom surface.

31. The method of claim 25 wherein the substrate has a planar bottom surface, with the first direction being oriented perpendicular to the planar bottom surface.

32. The method of claim 25 wherein each of the drift regions has a linearly graded doping profile.

33. The method of claim 25 wherein the insulating layer comprises silicon dioxide.